BHARAT ELECTRONICS LIMITED

(A Govt. of India Enterprise under the Ministry of Defence)

Product Development & Innovation Centre (PDIC) and Centre of Excellence (CoE)

Advertisement No. 6050/HR/PDIC/REC/SE/2024-25, dated: 28.04.2025

Bharat Electronics Limited (BEL) a Navaratna Company and Indian's premier Professional Electronics Company with a portfolio of over 350 different products in the areas of Military Communication, Radars, Naval Systems, C4I Systems, Weapon Systems, Homeland Security, Telecom and Broadcast, Electronic Warfare, Tank Electronics and Electro Optics.

Engineering Solutions, Antenna vertical, System on Chip design and CoE-Radar & Weapon Systems are few of the domain areas of PD&IC. Towards this, BEL invites applications from experienced outstanding professional for its "Product Development & Innovation Centre (PDIC) and Centre of Excellence (CoE), Bengaluru, for permanent post.

The details are as follows:

Sl. No.	Post / Grade	Job Code	Relevant/Required Education Qualification & Discipline	No. of Post(s)	Upper age limit as on 01.04.2025	Relevant post-qualification experience Industry/ Defence Laboratory experience as on 01.04.2025	CTC / Pay scale	Reservation/ No. of post(s)
1	Senior Engineer E-III (Physical Design Engineer)	**SOC01**	M.E/M.Tech in VLSI design/ Microelectronics	02	32 years	Minimum 2 Years	14 Lakhs (approx.)/ 50000-3%-160000	UR-2
2	Senior Engineer E-III	**ANT01**	B.E/ B.Tech in Electronics Engineering	01		Minimum 4 Years	14 Lakhs (approx.)/ 50000-3%-160000	UR - 05 EWS - 01 OBC - 03 SC - 02 ST - 01
3		**RWS01**	B.E/ B.Tech in Electronics Engineering	03				
4		**MEC01**	B.E/ B.Tech in Mechanical Engineering	08				

Relaxation will be extended as per Govt. guidelines in respect of Ex-Serviceman.

1.0 EDUCATIONAL QUALIFICATION:

i. **SENIOR ENGINEER (Physical Design Engineer):** Full time M.E/ M. Tech in VLSI design/ Microelectronics with First Class from an AICTE approved College/Institute or a recognized University.\

ii. **SENIOR ENGINEER:** Electronics /Mechanical Engineering discipline.

Full Time B.E/ B.Tech in relevant discipline with from an AICTE approved College/ Institute or a recognized University.

The Disciplines and subjects defined for the Engineering posts mentioned above are as follows:

SUBJECTS	DISCIPLINE
Electronics	Electronics Electronics & Communication Electronics & Telecommunication Communication Telecommunication
Mechanical	Mechanical Engineering

Please Note:

i. Applicants whose discipline/ specialisation mentioned in their Degree Certificates do not tally with the discipline/ specialisation prescribed in the advertisement will not be considered for selections.

ii. M.E/M.Tech or B.E/B.Tech Degree certificate (as applicable). **In case of CGPA or credits system of assessments, the candidates are required to attach the formula for conversion of CGPA/ Credits to percentage in accordance with the respective University norms.**

2.0 RELEVANT POST-QUALIFICATION INDUSTRY/ DEFENCE LABORATORY EXPERIENCE AS ON 01.04.2025:

"Candidates with specific experience as per the job responsibilities brought out will be considered for the job role. Prior experience as Trainees/ Fixed-tenure/ Contractual Engagement in BEL/ other PSUs will not be considered as relevant experience for the posts advertised".

2.1 JOB CODE: SoC01 (Physical Design Engineer)

I. Description:

- Responsible for creation of PD flows bring up/setup/flow flush, Timing analysis concepts.
- Planning for Timing Budgeting at system level and Constraints Development.
- Power Analysis and Estimation for the SoC.
- Responsible for Logical Synthesis, Physical synthesis, Place & route, Clock tree synthesis and timing closure for SoC designs.
- Responsible for STA setup, timing convergence, signoff for multi-mode, multi-voltage domain designs.
- Responsible for Physical Verification, collaborating with design and manufacturing teams to optimize the layout for the semiconductor fabrication process.

II. Essential:

- Good Knowledge on Chip integration, foundry PDK's, Tech files and Implementation level flow setup, top-down floor planning for sub-system/system level.
- Work experience on Die area estimation, Physical Partition of Sub-blocks, Shape & Pin Planning, power grid planning, channel planning and delivering top-down constraints for place and route. Optimizing the layout for Verification, DRC, LVS, density and power delivery.
- Good hands-on experience on Logical Synthesis, Physical synthesis, Place and route, Clock tree synthesis and timing closure at full chip and block level. Multiple Power Domain analysis using standard Power Formats UPF or CPF.
- Expertise on PD flows bring up/setup/flow flush, Understanding on Timing analysis concepts and Timing Budgeting at system level.
- Hands-on experience on Logical Synthesis, Physical synthesis, Place & route, Clock tree synthesis and timing closure.
- Experience on formal equivalency checks (LEC), LP, reliability, SI, and noise checks using sign-off tools.
- Experience in constraint development, validation and debug across multiple PVT conditions.
- Experience in automation scripts within STA/PD tools for methodology development. Performance
- optimization, including co-optimization work with process teams.
- Hands on experience in Design (DRC), Layout vs. Schematic (LVS) Verification, Electrical Rule Checking (ERC), Fill Insertion and Design for Manufacturing (DFM).
- Experience in addressing lithography and process variation concerns Rule Checking.

III. Desirable:

- Strong knowledge on Physical Design fundamentals and PnR cycle.
- Knowledge on Static timing analysis concepts.
- Knowledge on Post-Processing Simulation and Process Integration Checks.
- Strong knowledge in scripting languages (Perl, Tcl).
- Hands on experience with industry standard EDA Tool Flows: Cadence/ Synopsys/Mentor Graphics.

2.2 JOB CODE: MEC01

I. Essential:

- Experience in CAE -Structural / CFD Simulations.
- Experience in Simulation of Products/Systems in the areas of Research/ Design/ Development.
- Experience in Structural / thermal / Vibration / CFD flow simulations using CAE tools.

II. Desirable:

- Proficiency in one of the below areas,
  FEA: ANSYS/ MSC Nastran/ Altair.
  CFD: ANSYS Fluent/ CFX/ Star CCM+/Open Foam / Icepak
- Experience in Defence and Aerospace industries especially in the areas of Radar Systems, Missile Systems, Unmanned Platforms, Naval Systems, Stabilization Platforms is preferable.
- Knowledge and experience in Thermal Management simulations of Electronic Products/Systems. (Cold Plate, Fan Flow, Conduction, etc.)
- Knowledge and experience in Structural simulations of Electronic Products/Systems. (Static, Transient Structural, Modal, Frequency Response, Random Vibration, Explicit, Composites Simulations, etc.)
- Experience in analysis mitigation strategies for Vibration and Shock/ Base-excitation analysis/ Thermal / Coupled thermo-structural analysis etc.
- Experience in CFD (Computational Fluid Dynamics) simulations of turbulent flows, combustion modelling, Multi-phase flows, fluid structure interaction and External Aerodynamics.

2.3 JOB CODE: RWS01

I. Essential:

- Expertise in signal processing techniques such as Detection & estimation theory, Digital filter design, spectral estimation, DFT/FFT/DTFT/Z-transforms, time frequency transforms like STFT, wavelets, Joint time frequency transforms etc.
- Experience in knowledge of radar algorithms like Doppler processing, Constant False alarms (CFAR) for the radar types such as Pulse Doppler radars, FMCW radars, MIMO radars, Passive radars, Collision detection, and Foliage penetrating radars.
- Experience in the areas like Radar Beamforming techniques, Adaptive signal processing for DOA estimation and adaptive beam nulling etc.
- Knowledge in the areas like Linear algebra, vector calculus, 3D co-ordinate Geometry is added advantage.
- Domain knowledge in the high speed data acquisitions such as ADC/DAC mixed signal processing cards, RF ADC based designs, FPGA based hardware design. Understanding and awareness of DSP processor architectures such as RISC/CISC etc.

II. Desirable:

- Proficiency in algorithm development and simulation using C/C++ programming & MATLAB.
- Proficiency in VHDL/Verilog based algorithm development.
- Strong skills in developing and implementing algorithms on DSP from TI/Analog devices/ARM/PowerPC
- Strong skills in optimization and vectorization techniques of DSP algorithms.

2.4 JOB CODE: ANT01

I. Essential:

- Working experience in Design, Realization and Testing of Antennas from HF to Microwave Frequencies.

- strong theoretical and working level knowledge in design of Dipole, Log periodic, Bicone, Micro strip Patch, Waveguide Slot Antennas, Schematic Capture, PCB Design, Microwave Power Dividers and Microwave Amplifiers.
- Working Experience on Microwave CAD Tools such as CST Microwave Studio, Ansys HFSS, FEKO, Key sight ADS, MATLAB and AUTOCAD.
- Knowledge in PCB Design Tools such as Cadence Allegro.
- Knowledge in antenna testing and should be willing to take part in field trials on ground/sea platforms.

II. Desirable:

- Familiarity with design of Microwave Active circuits such as Amplifiers, Synthesizers etc
- Familiarity with Radome designs
- Familiarity with PCB Design Tools (such as Cadence Allegro, Altium) for Schematic Capture, PCB Design
- Familiarity with Design Tools such as MATLAB, AUTOCAD, Solidworks

Please Note:

- Only **relevant educational qualification** and relevant **post-qualification Industry/ Defence Laboratory** experience will be considered as per the advertisement.
- **Academy/ Teaching/ Apprenticeship/ Internship Training/ Research work experience** will not be considered as relevant post qualification/ industrial experience. Prior experience as Trainees/ Fixed-tenure/ Contractual Engagement in BEL/ other PSUs will not be considered as relevant experience for the posts advertised
- The decision of the selection committee, with respect to relevance of experience and selection of candidates in will be final. Work experience indicated without supporting documents, will not be considered.
- Candidates are requested to read the advertisement in details & apply to the most suitable job code.

3.0 UPPER AGE LIMIT & RELAXATION:

As on **01.04.2025** the upper age limit for the post of Sr. Engineer (E-III) is 32 Years.

The upper age limit will have relaxation for OBC(Non–Creamy Layer) candidates by 03 years and SC/ST candidates by 05 years. For candidates belonging to Persons with Benchmark Disability (PwBD) category having minimum 40% disability or more will get 10 years relaxation in upper age limit in addition to the relaxation applicable to the categories mentioned above. Relaxation will be extended as per Govt. guidelines in respect of Ex-Serviceman.

4.0 REMUNERATION:

Senior Engineer (E-III) -

Pay scale Rs. 50,000-3%-1,60,000, in addition to Basic Pay, other allowances like Dearness Allowance, House Rent Allowance, 35% of the Basic Pay as perquisites, Performance Related Pay (PRP), Group Insurance, Medical facilities and Provident Fund as per the Company's rules will be part of the remuneration package.

5.0 SELECTION PROCEDURE:

a. Candidates have to carefully enter the details in the application and attach the documents as prescribed. In case, the details mentioned do not tally with supporting documents, the candidate's application will be rejected without any prior intimation.

b. Candidates meeting the eligibility criteria as stipulated in the advertisement will be shortlisted based on scrutinizing of the application and called for the Written Test followed by interview for candidates.

c. Based on the Written Test score, candidates will be shortlisted for interview in the order of merit in the ratio 1:5 category wise. The Interview will be conducted for 15 marks.

d. The list of candidates shortlisted for the Written Test/Interview will be posted on the BEL Website. Candidates are required to comply with the instructions indicated in the Admit Card.

e. The venue for the Written Test/Interview will be at BEL, Bengaluru.

6.0 FEE PAYMENT:

a. Candidates are required to remit an amount of Rs. 600/- plus 18% GST towards application fee through SBI Collect (through online mode or through SBI Branch). SC/ST/PwBD/Ex-Servicemen candidates are exempted from payment of application fee.

b. Candidates are required to read the details and screenshots for making the payment.
c. Candidates can also make the payment by approaching SBI branch. Candidates are required to select SBI branch in the payment option and download & print the challan generated through SBI Collect and deposit the application fee of Rs. 600/- plus 18% GST applicable bank charges in any SBI Branch. The candidate should ensure to obtain the seal and signature of the bank official.
d. Candidates have to enter the "**SBI Collect Reference No.**" generated after payment, in the Application Form. SC/ST/PwBD candidates are exempted from payment of application fee.
e. Candidate may go through all instructions and eligibility criteria carefully before remitting application fees and sending the application. **Fees once paid will not be refunded under any circumstances**. Candidates may take note that no cheque, DD or cash will be accepted towards payment of application fee.

INSTRUCTION FOR MAKING PAYMENT:

a. Go to www.onlinesbi.com and select:- State Bank Collect.
b. Accept Terms and Conditions and click on "**Proceed"**.
c. Select state of Corporation/ Institution: - All India.
d. Select type of Corporation/ Institution: - PSU – Public Sector Undertaking and Click on "**Go"** option.
e. Select PSU - Public Sector Undertaking: - Bharat Electronics Limited and Click on "**Submit"** button.
f. Select Payment category: - **Senior Engineer (E-III) Post - "Recruitment of Senior Engineer (E-III)"**
g. Complete the payment as explained above
h. Take a print of the payment receipt and mandatorily attach it with the application form where applicable.

Note: While paying application fees through SBI collect, candidates should ensure that they mention the same mobile number and email id in SBI collect as has been mentioned by them in the application form.

7.0 GENERAL INSTRUCTIONS:

a. Internal candidates of BEL are not eligible to apply.
b. The Cut-off date for deciding the maximum permissible age and experience (Post-Qualification Experience Industry/ Defence Laboratory experience) shall be **01.04.2025.** In order to compute post-qualification work experience, the period of work experience starting from the month immediately succeeding the month of final examination in which candidate acquire the essential educational qualification shall be considered.
c. Candidates working in PSUs/ Government/ Quasi Government organizations should compulsory produce "**No Objection Certificate**" at the time of the interview. Such candidates, who are unable to produce NOC at the time of interview, will not be considered for interview.
d. Candidates are required to travel extensively anywhere in India.
e. Outstation Candidates called for interview shall be reimbursed III Tier AC fare for Senior Engineer to and fro train fare by the shortest route (from their correspondence address) on production of receipt or other supporting documentary evidence in respect of the onward journey.
f. Request for change of category once declared in the application will not be entertained.
g. The exact date and time shall be communicated in the Admit Card for Written Test. Candidates are required to possess at least one valid e-mail id which is to be entered in the application form. Information pertaining to the Written Test/ Interview will be sent by e-mail to the id that is furnished and also will be published in the BEL Website. BEL will not be responsible for bouncing of any e-mail sent to the candidate.
h. In the event any applicant has litigated with his/her employer in the past, the same should be clearly mentioned in brief.
i. The Disability Certificate should be strictly in the format available on the BEL website.
j. The number of posts indicated above may vary based on the actual requirement at the time of selection.
k. Canvassing in any form will result in disqualification.
l. Only Indian nationals need to apply.
m. Merely fulfilling the minimum requirement of qualification and experience will not vest any right on the candidates to be called for the Interview/Written Test. The admission at all / any stage of selection process will be purely provisional. Mere issue of admit card / interview call letter/provisional offer of appointment to the candidate will not imply that his / her candidature has been cleared by BEL.
n. Interested candidates meeting all the criteria mentioned aloft, should submit the application in the format appended to this advertisement and send the applications through post, super-scribing on the envelope the post applied for.

The following documents should compulsorily be enclosed along with application:

- Self-attested copy of SSLC/Matriculation Certificate (proof of age).
- Self-attested copy of PUC/12th Class/Diploma Marks Card.
- Self-attested copies of Degree Marks cards for having passed all semesters/years.
- Self-attested copies of Provisional/Final Degree Certificate.
- Conversion formula certificate for conversion of CGPA to percentage, duly certified by the University/ Institution, wherever applicable.
- Post qualification experience certificate(s) from previous to till current employer. The joining/appointment letter and relieving letter (wherever applicable) needs to be attached to determine the number of years of post-qualification experience. Where current employment certificate is not produced the joining/appointment letter, first and latest pay slip and employee ID proof should be **compulsorily** attached to determine the number of years of experience. In case of failure to enclose the supporting documents your application will be summarily rejected without assigning any reason and no correspondence in this regard will be entertained.
- Category/ Tribe/ Community/ Disability/ Economic status certificate in case of candidates belonging to SC/ ST/ OBC/ PwBD/ EWS respectively. Candidates claiming reservation under any of the above categories are required to submit the certificate in the prescribed format. **The formats of various certificates are provided as link to the advertisement**. Candidates belonging to OBC category should produce the certificate issued on or after **01.04.2024** and candidates belonging to EWS must produce a valid income and Asset Certificate.
- Candidates if working in PSUs/ Govt. organizations/ Quasi Government organisations should compulsorily submit '**No Objection Certificate**' at the time of application or interview.
- SBI Fee Payment Receipt (if applicable).
- **Write up of the roles and responsibilities/ experience**, **mandatorily to be attached**.

o. Failure to forward the indicated enclosures will result in disqualification, even if the candidates have remitted the application fee.

p. Any revision, clarification, addendum, corrigendum, time extension etc. to the above advertisement will be hosted on the careers section of BEL website and no separate notification will be issued in the press.

BEL reserves the right to debar / disqualify any candidate at any stage of the selection process for any reason what so ever and also reserves the right to cancel / restrict / enlarge / modify or alter the recruitment or selection process, if need so arise without issuing any further notice or assigning any reason thereafter.

Candidates are advised to visit the website regularly to keep themselves updated.

Applications complete in all respects should be sent by Indian post (sealed envelope-A4 size) only.

Super-scribed for Senior Engineer (E-III) "**Application for the post of Senior Engineer (Job Code No.: _____)**" and sent to below mentioned address:

Deputy General Manager (HR),
Product Development & Innovation Centre (PDIC),
Bharat Electronics Limited,
Prof. U R Rao Road, Near Nagaland Circle,
Jalahalli Post, Bengaluru – 560 013, India.

The application should reach the given address **on or before 19.05.2025 through registered Post only**, any applications received after the closing date **will not be considered**. Application that are incomplete, not in the prescribed format, not eligible, without the required enclosures and received through other means than Indian Post will be summarily rejected without assigning reasons and no correspondence in this regard will be entertained.

There will be no separate communication to any candidates on their non-selection at any stage.

For clarification if any in respect of the above advertisement, you may write to **hrpdicrec@bel.co.in** or contact on 080-2219 5211(during working hours between 09.00 am to 04.00 pm).

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